

METHOD FOR FORMING A DUAL DAMASCENE STRUCTURE
IN A SEMICONDUCTOR DEVICE

Field of the Invention

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The present invention relates to a method for manufacturing a semiconductor device; and, more particularly, to a method for forming a dual damascene structure in a semiconductor device.

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Background of the Invention

As an integration of a semiconductor device goes on, a research on a capability enhancement of the semiconductor device as well as down sizing thereof is performed at the same time. At present, most wiring structure of the semiconductor device adopts a multi-layer wiring structure. The multi-layer wiring structure may overcome problems on signal transmission speed that are generated during an operation of highly integrated device. And with an advent of the multi-layer wiring structure, a dual damascene process is highlighted due to its simplicity. The dual damascene process is composed of the steps of forming a contact hole and a trench in an insulating layer, performing a gap-fill on a conductive film, and performing a chemical mechanical polishing to thereby form a wiring and a contact

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hole at the same time.

There are several methods for forming a dual damascene structure in a semiconductor device. One of a conventional methods is shown in Figs. 1A to 1D. Two photolithographic processes and two insulator layers separated by an etch stop layer are employed to achieve the shown structure as follows. In this method, the dual damascene structure is formed by a way that a trench is first formed and then a contact hole is formed in an insulating layer later.

As shown in Fig. 1A, a semiconductor substrate 10 is provided with a semiconductor device (not shown) therein. Thereafter, a first etch stop layer 12 is applied on the semiconductor substrate 10. And then, a first insulating layer 14, a second etch stop layer 16 and a second insulating layer 18 are deposited on the first etch stop layer 12 sequentially. And then, a first photoresist pattern 20 for defining the trench is formed on the second insulating layer 18 by a photolithography process.

And, as shown in Fig. 1B, the second insulating layer 18, in turn, is etched down to the second etch stop layer 16 so that a trench 18a is formed and then the first photoresist pattern layer 20 is removed.

And then, as shown in Fig. 1C, a second photoresist layer 22 for defining a contact hole 24 is applied on the trench 18a.

Thereafter, as shown in Fig. 1D, the second etch stop

layer 16 and the first insulating layer 14 defined by the second photoresist pattern 22 is etched so that the contact hole 24 can be formed. In another embodiment, the first etch stop layer 12 may also be etched down to expose a portion of the semiconductor device, such as a wiring or an activated area, although it is not shown in Fig. 1D. Thereafter, the second photoresist pattern 22 is removed to complete a dual damascene structure.

Another conventional method for forming a dual damascene structure is presented in Figs. 2A to 2D, in which a contact hole is first formed in an insulating layer and then a trench is formed.

As described in Fig. 2A, a semiconductor substrate 30 is provided with a semiconductor device therein. Thereafter, a first etch stop layer 32 is applied on the semiconductor substrate 30. And then, a first insulating layer 34, a second etch stop layer 36 and a second insulating layer 38 are deposited on the first etch stop layer 32 sequentially. And then, a first photoresist pattern 40 for defining a contact hole is formed on the second insulating layer 38 by a photolithography process.

And, as shown in Fig. 2B, the second insulating layer 38, the second etch stop layer 36 and the first insulating layer 34 are etched down so that a contact hole 42 is formed. And then the first photoresist pattern layer 40 is removed. In another embodiment, though it is not shown in Fig. 2B,

the contact hole 42 uncovering a portion of a semiconductor device may formed by etching the first etch stop layer 32.

And then, as shown in Fig. 2C, a second photoresist layer 44 for defining a trench 48 is applied on the second insulating layer 38a. At this time, a gap filler 46 for filling the contact hole 42 up to the second etch stop layer 36a is formed in order to protect the semiconductor device when the second insulating layer 38a is etched.

Thereafter, as shown in Fig. 2D, the second insulating layer 38a defined by the second photoresist pattern 44 is etched to form the trench 48 for wiring. Then, the second photoresist pattern 44 and the gap filler 46 are removed to complete the dual damascene structure.

Still another conventional method for forming a dual damascene structure is shown in Figs. 3A to 3D. In this method, the dual damascene structure is formed by a way that a trench for wiring and a contact hole are formed by a self-aligned process.

As described in Fig. 3A, a semiconductor substrate 50 is provided with a semiconductor device therein. Thereafter, a first etch stop layer 52 is applied on the semiconductor substrate 50. And then, a first insulating layer 54 and a second etch stop layer 56 are deposited on the first etch stop layer 52 sequentially. And then, a first photoresist pattern 58 for defining a contact hole is formed on the second etch stop layer 52 by a photolithography process.

And, as shown in Fig. 3B, the second etch stop layer 56, in turn, is etched to form a patterned second etch stop layer 56a and then the first photoresist pattern layer 58 is removed.

5 Sequentially, as shown in Fig. 3C, a second insulating layer 60 is applied on the structure of Fig. 3B and a second photoresist layer 62 for defining the trench for wiring is applied on the second insulating layer 60.

 And then, as shown in Fig. 3D, the second insulating
10 layer 60 defined by the second photoresist pattern 62 is etched and at the same time the first insulating layer 54 also is etched by using the patterned second etch stop layer 56a in a self-aligned way to form a dual damascene contact hole 64. Thereafter, the second photoresist pattern 62 is
15 removed to complete the dual damascene structure. In another embodiment, though it is not shown in Fig. 3D, the first etch stop layer 52 may be etched so as for the underlying semiconductor device to be exposed.

 Therefore, it is evident that the process is
20 complicated, especially in that two photoresist processes must be used to form the trench and contact hole patterns. The multiplicity of the processes results in a lower productivity, and an increased cost.

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Summary of the Invention

It is, therefore, an object of the present invention to provide a method for forming a dual damascene structure in a semiconductor device by using single photolithography process and single etch stop layer.

In accordance with a preferred embodiment of the present invention, there is provided a method for forming a dual damascene structure in a semiconductor device, the method comprising the steps of: providing a substrate having a structure thereon; forming an insulating layer and an etch stop layer on the substrate sequentially; forming a first opening pattern for exposing a part of an upper surface of the etch stop layer by using a photolithography process; etching the etch stop layer by transferring the hole pattern into the etch stop layer; forming a first opening by etching the insulating layer down to a predetermined depth by transferring the hole pattern into the insulating layer; performing a pull back etching of an upper and side surface of the etch stop layer by a predetermined thickness for defining a second opening pattern; and forming a second opening and a third opening in the insulating layer by etching the etch stop layer and the insulating layer until the etch stop layer is removed, wherein the second opening and the third opening are etched by using the second opening pattern and the first opening as a mask, respectively.

Brief Description of the Drawings

5 The above and other objects and features of the present invention will become apparent from the following description of a preferred embodiment given in conjunction with the accompanying drawings, in which:

10 Figs. 1A to 1D show a sequence of a conventional method for forming a dual damascene structure in a semiconductor device;

Figs. 2A to 2D present a sequence of another conventional method for forming a dual damascene structure in a semiconductor device;

15 Figs. 3A to 3D offer a sequence of still another conventional method for forming a dual damascene structure in a semiconductor device; and

20 Figs. 4A to 4D illustrate a sequence of a method for forming a dual damascene structure in a semiconductor device in accordance with the present invention.

Detailed Description of the Preferred Embodiments

25 The preferred embodiment of the present invention will now be described in detail with reference to the accompanying drawings.

Figs. 4A to 4D show a method for forming a dual

damascene structure in a semiconductor device in accordance with the present invention.

A semiconductor substrate 100 in Fig. 4A is provided with metal layers for a semiconductor device therein. And
5 then an insulating layer 102 is deposited preferably using silicon oxide on the semiconductor substrate 100, although it may alternatively be formed of another insulating material, for example BPSG (borophosphosilicate glass), USG (undoped silicate glass), or FSG (fluorinated silicate glass).
10 It is preferred that the insulating layer 102 are deposited by plasma enhanced chemical vapor deposition or high-density plasma deposition and has a thickness of about 4000 to 8000 angstroms(Å).

Thereafter, an etch stop layer 104 containing such as
15 silicon nitride (SiN) is applied on the insulating layer 102. Other etch stop materials such as an oxide, a nitride or a polysilicon are also suitable. A thickness of the etch stop layer 104 is determined by that of the insulating layer 102 to be etched in succeeding etching processes. It is
20 preferred that silicon nitride is deposited using a low pressure chemical vapor deposition and that it has a thickness between about 500 to 2000 angstroms(Å).

Then, a photoresist pattern 106 is formed on the etch stop layer 104 to define a first opening pattern. And then,
25 a part of the etch stop layer 104 is removed by using a etching performed in accordance with an etching recipe

comprising Ar at a flow rate about 500 sccm, O₂ at about 10 sccm, and CH₂F₂ at about 20 sccm under a process pressure of about 150 mTorr, a source power of about 1000 W, and a temperature of about 20 °C so that a part of the insulating layer 102 is exposed. The etching process time is determined by the thickness of the etch stop layer 104. After the insulating layer 102 is exposed, the photoresist pattern 106 is removed.

Sequentially, as shown in Fig. 4B, a first opening 108 is formed by a dry etching over the exposed insulating layer 102. Herein, the first opening 108 is formed to have a predetermined depth into the insulating layer 102 and the etching processing is controlled in order for the insulating layer 102 below the first opening 108 to have a enough thickness for succeeding etching processes. The depth of the first opening 108 into the insulating layer 102 is determined based on the thickness of the insulating layer 102. It is preferred that the first opening 108 is formed by using an oxide etching recipe comprising Ar at a flow rate about 380 sccm, O₂ at about 10 sccm, CO at about 300 sccm, and C₄F₈ at about 16 sccm under process pressure of about 55 mTorr, a source power of about 1700 W, and a temperature of about 20 °C. The etching process time is determined by the thickness of the insulating layer to be etched.

And then, as shown in Fig. 4C, the etch stop layer 104

is striped partially by a wet etching an upper and lateral surface thereof. Dot lines in Fig. 4C indicate a portion of the upper and lateral surface of the etch stop layer 104 which is removed by the wet etching. The wet etching is performed by using a pull back etching in the atmosphere of H_3PO_4 at temperature of about 160 °C. The pull back etching is operated until the etch stop layer 104 is striped to expose a specific area of the insulating layer 102, wherein the specific area is corresponding to a place where a wiring for device is disposed. That is, the etched portion of the etch stop layer 104 is determined by a design rule for wiring to be constructed in a trench of the dual damascene structure.

Thereafter, as shown in Fig. 4D, the rest etch stop layer 104a and the insulating layer 102 is etched by using the same etching recipe which has used for forming the first opening. Through this etching process, a side wall and a bottom area of the first opening 108 is etched to form a second opening 110 and third opening 112. That is, the rest etch stop layer 104a serves as a mask for the second opening 110 and the first opening 108 serves as a mask for the third opening 112. This etching proceeds until the rest etch stop layer 104a is removed on the upper surface of the insulating layer 102. Therefore, the second opening 110 is broader than the third opening 112 and the etch stop layer 104 is removed. That is, the upper surface of the insulating layer

102 serves as an end point for the etching and the insulating layer 102 is etched with the etch stop layer 104 at the same time.

Herein, the etching ratio between the etch stop layer
5 and the insulating layer to be etched by the above oxide etching is about 1:10 to 1:30. The etching ratio may vary according to the material composing the etch stop layer and the insulating layer. For example, if the etch stop layer is composed of a nitride layer and the insulating layer is
10 composed of an oxide layer, the etching ratio is about 1:20. In this case, the rest etch stop layer 104a on the insulating layer 102 of 300 angstroms is enough to etch down the insulating layer 102 down to 6000 angstroms. As described above, the rest etch stop layer 104a serves as the
15 end point of an etching.

The second opening 110 may be used for the contact hole whereby a wiring interconnections are disposed, and the third opening 112 may be used for the contact hole having a contact with the underlying metal layers.

20 Therefore, a dual damascene structure can be made by using single photoresist process and single etch stop layer so that a forming process for the dual damascene structure is simplified.

While the invention has been shown and described with
25 respect to the preferred embodiments, it will be understood by those skilled in the art that various changes and

modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.